TEC-602 1093

Even Semester Examination 2018-19

B.Tech.(EEE/EN) (SEMESTER-VI)

VLSI CIRCUIT DESIGN

Time: 03:00 Hours **Max Marks :100**

Note :All questions are **compulsory**. Draw diagrams wherever necessary. All questions **carry equal** marks. .

1. Attempt **any four** parts of the following : [5×4=20]

   (A) Explain the basic organization of N-MOS NAND ROM and its layout.

   (B) Explain CMOS SRAM cell with a neat diagram.

   (C) Draw the typical architecture of PLA.

   (D) Implant the following logic function using a 2^2 X 3 bit ROM :

   $X = AB$

   (E) Explain the data programming and erasing methods in flash memory with its suitable diagrams.

   (F) What are FPGAs? Explain its principle and operation.

2. Attempt **any four** parts of the following : [5×4=20]

   (A) Explain the Built-In Self-Test (BIST) techniques for VLSI circuit testing.

   (B) Explain Sensitized Path-Based Logic Testing with a suitable example.

   (C) Define the term Controllability and observability.

   (D) Explain the different kind of physical defects (Faults) that can occur in a CMOS circuit.

(E) What are the Scan Design Techniques? Explain in brief.

(F) Write a short note on Testing Sequential Logic.

3. Attempt **any two** parts of the following : [10×2=20]

(A) Derive an equation for trans-conductance of an n-channel enhancement MOSFET operating in active region.

(B) Explain the process sequence for CMOS integrated circuit fabrication with the help of neat diagram.

(C) Discuss the operation of pass transistor in dynamic logic circuit. Draw the BICMOS inverter circuit.

4. Attempt **any two** parts of the following : [10×2=20]

(A) Explain the DC characteristics of CMOS inverter with its region of operation.

(B) Consider a CMOS inverter circuit with the following parameters V_{DD} =3.3 V, V_{Ton} = 0.6V, V_{Top} = –0.7 V, μnCox = 60 μA/V^2, (W/L)n = 8, μpCox = 20 μA/V2, (W/L)p=12. Calculate the noise margin of the circuits.

(C) How switch logic circuit can be implemented using pass transistors? Explain it in detail.

5. Attempt **any two** parts of the following : [10×2=20]

(A) Discuss the operation of single stage shift register circuit. Design a SR flip-flop using CMOS circuit.

(B) Design the circuit described by the Boolean function $Y = \overline{A(B+C)(D+E)}$. Using CMOS logic.

(C) (i) Starting from the truth table, design a gate level and transistor level clocked JK latch circuit.

(ii) Draw the basic building block of a CMOS transmission gate dynamic shift register and explain its working.

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