TEC-602 263

Even Semester Examination 2017-18

B.TECH (SEMESTER-VI)

V L S I CIRCUIT DESGN

Time: 03:00 Hours **Max Marks : 100**

Note: Attempt ALL question. All Question carry equal marks.

Q1. Attempt any four parts of following: **(5x4=20)**

(A) Explain the threshold voltage of a MOS device and explain its significance?

(B) What are the advantages of BICMOS technology over CMOS technology?

(C) Explain the fabrication steps for CMOS using Twin Tub technology?

(D) Explain the VLSI design flow and explain each block?

(E) Explain electrical properties of MOS and derive various equations for it.?

(F) What is pass transistor? Explain with suitable example also implement Half adder circuit by NMOS Pass Transistor logic?

Q2. Attempt any four parts of following: **(5x4=20)**

(A) Derive expression of power dissipation in CMOS Inverter?

(B) Explain Lambda design rule and its physical significance in VLSI domain?

(C) Derive expression for pull-up to pull-down ratio for NMOS inverter driver by another NMOS inverter?

(D) F= {A.(D+E)+B.C}' Realize this function using CMOS technology?

(E) Discuss the architecture and advantages of FPGA? What are the different type of Xilinx FPGA?

(F) Describe the channel length modulation in the MOSFET?

Q3. Attempt any two parts of following: **(10x2=20)**

(A) Derive DC Characteristic of CMOS Inverter? Derive it Voltage and current equation?

(B) Explain the concept of Pipelining and Timing issues in VLSI Circuit?

(C) Implement NAND and NOR gate having two input with CMOS logic?

Q4. Attempt any two parts of following: **(10x2=20)**

(A) Implement BCD to gray code converter using PLA?

(B) Explain the operation of 6-Transistor SRAM with proper circuit diagram? Also write difference between DRAM & SRAM?

(C) Define the term Controllability and Observability for VLSI circuits with examples?

Q5. Attempt any two parts of following: **(10x2=20)**

(A) Discuss briefly testing and verification of VLSI Circuits?

(B) Explain in details Built in self-Testing (BIST) for circuit testing in VLSI?

(C) What do you mean by electrical logical Stuck-at-0 & stuck-at-1 faults, explain with suitable examples?

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