TEC-602 202 Printed Pages : 4

Paper Code & Roll No. to be filled in your Answer Book

Roll No. | | | | | | | | | | |

B.Tech. (VI - Sem.)

Even Semester Examination - 2016

VLSI CIRCUIT DESIGN

[Time : 3 Hours] *[Maximum Marks :100]*

Note: Attempt **all** questions. Assume data wherever necessary.

1. Attempt **any four** parts of the following: (5x4=20)

   (a) Explain MOS capacitor under external bias conditions and also draw capacitance –voltage curve for MOS capacitor with P-type semiconductor as substrate material?

   (b) Explain the threshold voltage of a MOS device and explain its significance?

   (c) What are the advantages of BICMOS technology over CMOS technology? Also implements NOT gate by using BICMOS technology?

   (d) What is pass transistor? Explain with suitable example also implements half adder circuit by using NMOS pass transistor logic?

(e) Explain constant-voltage scaling & constant-field scaling of MOSFET?

2. Attempt **any four** parts of the following : (5x4=20)

(a) Describe CMOS transmission gate (CMOS TG) as a constant resistive element for logic '1' transfer?

(b) Implements full adder by using CMOS logic technology? Also draw the coloured stick diagram for 2-inputs NOR gate?

(c) Derive expression for pull-up to pull-down ratio for NMOS inverter driven by another NMOS inverter?

(d) Derive an expression for calculation of rise time and fall rise of a CMOS inverter?

(e) Describe the concept of noise margin for CMOS inverter? Calculate the noise margin of CMOS inverter with $V_{DD}=5V, V_{T,P}=-1V, V_{T,N}=1V, K_N=210\mu A/V^2$ & $K_p=210\mu A/V^2$?

3. Attempt **any two** parts of the following: (10x2=20)

(a) Draw and explain the SR latch using CMOS logic design and based on NOR gate? Also draw the coloured stick diagram for above SR latch circuit?

(b) Explain structure and operation of 'D' flip-flop by using CMOS technology with minimum no. of transistor? Also writes its applications?

(c) A function is given as below:

$F=[A.(D+E)+B.C]'$

(i) Realize this function using CMOS technology?

(ii) Draw the coloured layout diagram for above CMOS logic circuit in part (i)?

4. Attempt **any two** parts of the following: (2x10=20)

(a) Explain the operation of 6-Transistor SRAM with circuit diagram? Also writes difference between DRAM & SRAM?

(b) Discuss the different applications and advantages of FPGA? What are the different of simple Xilinx FPGA?

(c) Design and implement the following multiple output combinational circuits using PAL:

(i) $Z=A'.B.C.D'+A'.B.C'.D+B.C.D'+A.B'.D'$

(ii) $Y=A.B.C.D'+A'.B.C'.D+B.C.D'+A.B'.D'$

5. Attempt **any two** parts of the following: (10x2=20)

(A) (i) Define the terms Controllability and observability for VLSI circuits with example?

(ii) Explain concepts of pipelining?

(B) (i) What do you mean by electric logical stuck-at-0 & stuck-at-1faults, explain with suitable example?

(ii) Explain in details Built-in self testing (BIST) for circuit testing in VLSI?

(C) Derive the expression for channel length modulation? Consider an n-channel MOSFET that measured to have I_{DS}= 100μA and V_{GS}=2V, V_{DS}=3V in first case and then consider I_{DS}= 104μA and V_{GS}=2V, V_{DS}=4V in second case. Calculate the Value of channel length Modulation index (λ).

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