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Roll No. to be filled in your Answer Book

Roll No. | | | | | | | | | | | |

B. Tech. (Electronic & Communication)
(6TH Semester) Examination, 2015
VLSI Circuit Design

Time: 3.00 Hrs] **[Max. Marks: 100**

Note: Attempt All Questions. All Questions carry equal marks.

Q1. Attempt any four of the following:- 4X5=20

a) Describe the electrical properties of BICMOS structure.

b) What do you understand by latch? Draw the layout of a latch.

c) Explain the design rules in VLSI.

d) What do you understand by scalling? what are the size reduction strategies for MOSFET?

e) Explain concept of pipelining.

f) Write the notes on Sequential MOS logic circuit.

Q2. Attempt any four parts of the following:- 4X5=20

a) Design a 2 input AND gate using CMOS as well as Pass transistor and compare the number of transistors.

b) Design a 2XI MUX with help of CMOS transmission gate and explain its working.

c) Compare FPGA and CPLD.

d) Describe Built -In Self Test (BIST) technique.

e) Explain the MOS transistor transconductance (g_m) and output conductance (g_{ds}).

f) A MOS system is under external bias. Explain the different operating region and Threshold Voltage.

Q3. Attempt any two parts of the following:- 2X10=20

a) Calculate the threshold voltage V_{tO} at V_{SB}=0, for a polysilicon gate n-channel MOStransistor, with the following parameters:

Substrate doping density $N_A = 10^{16} cm^{-3}$, Polysilicon gate doping density $N_D = 2 X 10^{20} cm^{-3}$, gate oxide thickness $t_{ox} = 500A°$ and oxide -interface fixed charge density $N_{ox} = 4X10^{10} cm^{-2}$

b) Define the delay time .Calculate the delay time for CMOS invertors using average delay time method and differential equation methods.

c) (i) Explain the programmable logic structure available in PAL.

(ii) Describe a PLA in brief.

Q4. Attempt <u>any two</u> parts of the following:- 2X10=20

a) Describe the structure and operation of MOSFET with its characteristics.

b) A function is given as below-

$$F = \overline{A(D+E) + BC}$$

(i) Realize this function using NMOS.

(ii) Draw the CMOS stick- diagram layout of this function.

c) Determine pull up and pull down ratio for an NMOS inverter driven by another NMOS inverter.

Q5. Attempt <u>any two</u> parts of the following:- 2x10=20

a) Calculate the critical voltage (V_{OL} V_{OH}, V_{IL}, V_{IH}) and find out the noise margin of the depletion -load inverter circuit whose parameters are as-

V_{DD}=5 V, $V_{TO,Driver}$=1.0 V, $V_{TO,Load}$= -3.0V, $(W/L)_{driver}$=2, $(W/L)_{load}$=1/3,

$K'_{n,driver}=K'_{n,load}=25\mu A/V^2$, γ =0.4 $V^{1/2}$, Φ_F=-0.3 V.

b) Describe DRAM and SRAM semiconductor memories.

c) Explain with diagram the design strategies for testing the CMOS devices.

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