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**TEC-302**

**Roll No.** | | | | | | | | | | |

# ODD SEMESTER EXAMINATION 2019-20
## B. TECH III SEM (Old Syllabus)
## DIGITAL ELECTRONICS & DESIGN ASPECTS

**[Time: 3 HOURS]** **[Total Marks: 100]**

**Total no. of printed pages: 3**

**Attempt all the questions. All questions carry equal marks**

**Q1. Attempt any four parts of the following:** **( 5*4)**

a) Determine the base 'b' in each of the following cases:
   (a) $(361)_{10} = (551)_b$
   (b) $(859)_{10} = (5B7)_b$

b) Define Hamming code of error detection. Obtain 7-bit Hamming code for the message signal 1101 by using even parity.

c) Using K-Map simplify the following expression:
   $F(A, B, C, D) = \sum_m (0,1,3,7,9,11,12) + \sum_d (2,4,10)$

d) Subtract the following numbers by using 2's complement method:
   i) $(1101)_2 - (1011)_2$
   ii) $(791)_{10} - (483)_{10}$

e) Define minterms and maxterms with examples.

f) Convert the following expressions to the canonical form:
   i) $F = AB' + A'C + A$
   ii) $F = (A + B)(B' + C)$

**Q2. Attempt any four parts of the following:** **(5*4)**

a) Implement the following function by using 4:1 Mux
   $F(A, B, C) = \sum_m (0,1,3,6)$

b) Explain the working of 3:8 Decoders.

c) Explain with an example the differences between PLA & PAL.

d) Design a 4-input combinational circuit that converts binary code to gray code.

e) Obtain Boolean expression for the outputs of a 4-input magnitude comparator.

f) What are the drawbacks of a full adder? Explain how a parallel adder removes the drawback of a full adder?

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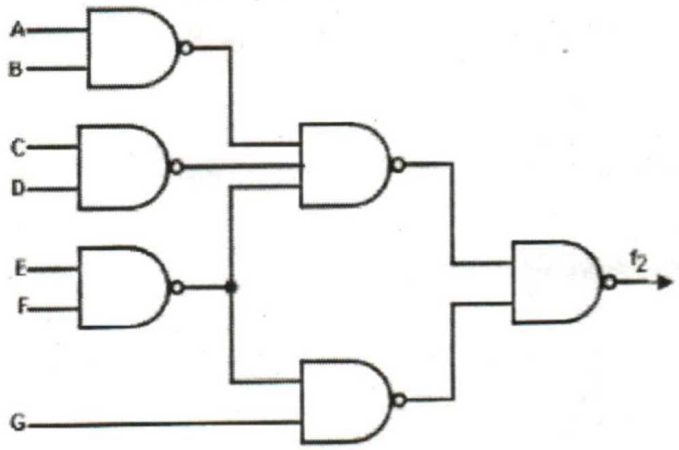
**Q3. Attempt any two parts of the following:** **(10*2)**

a) What is Race-Around condition? Explain the master-slave JK flip-flop.

b) Analyze the circuit shown in fig. 1 to produce Boolean algebraic expression for the circuit outputs.




c)

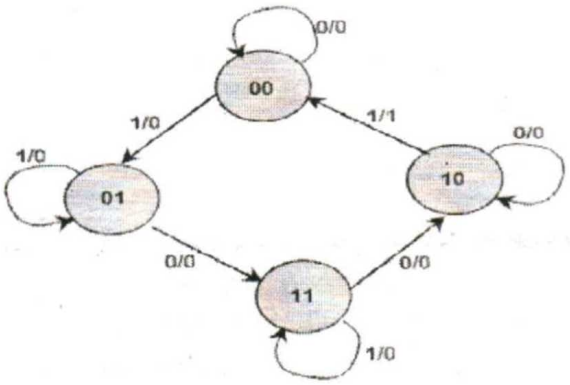
d) **Fig. 1**

(c) With the help of timing diagram, explain the working of a Mod-6 ripple counter if Flip-Flop used is negative edge triggered JK Flip-Flop.

**Q4. Attempt any two parts of the following:** **(10*2)**

(a) With the help of neat and clean diagram explain the working of TTL NAND gate. Write the comparative table of various logic families.

(b) For the following state diagram, design the synchronous sequential circuit by using D Flip-Flip:




(c) Design D Flip-Flop and T Flip-Flop by using SR Flip-Flop.

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**Q5. Attempt any two parts of the following:** **(10*2)**

a) Differentiate between the working of static and dynamic memory. Also discuss the difference between SRAM and DRAM.

b) Explain static and dynamic hazards with suitable examples. Use a digital circuit of your choice and show how hazard is removed to obtain a hazard free circuit.

c) Write short note on any four of the following:

I. Random Access Memory.
II. Tri-state Logic
III. MUX
IV. EPROM
V. Don't care condition

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