TCS-401/TIT-401 1024/1025

**Even Semester Examination 2018-19**

**B. TECH. (ECE/CSE/IT) (SEMESTER-IV)**

# COMPUTER ORGANIZATION

**Time: 03:00 Hours** **Max Marks :100**

**Note** : A, B, C, D, and E are the five sections in the question paper. Attempt four parts from A, four parts from B, four parts from C, two parts from D, and also two parts from the section E.

## SECTION A

Attempt **any four** questions from the following. Each question carries **equal** marks.

[4x5=20]

1. What is bus? Draw and describe the bus architecture for a digital computer.
2. State the differences between serial and parallel transmission.
3. What is a Von Neumann architecture? Also, discuss the Von Neumann bottleneck.
4. Discuss your understanding of stack memory.
5. Apply Booth's algorithm to multiply the two numbers $(6)_{10}$ and $(-9)_{10}$ . Assume the multiplicand and multiplier to be 5-bits each.

## SECTION B

Attempt **any four** questions from the following. Each question carries equal marks.

[4x5=20]

1. Define the cache memory along with its significance.
2. Differentiate between write-through and write-back mechanism.
3. Briefly explain the IEEE 754 standard format for floating point representation.

4. State the differences between instruction-pipeline and arithmetic-pipeline.

5. What are the priority interrupts? Briefly explain any one interrupt priority scheme.

## SECTION C

Attempt **any four** questions from the following. Each question carries equal marks.

[4x5=20]

1. With a neat and clean diagram, explain the internal organization of a 2M x * dynamic memory chip.

2. Perform the following operation on the 5-bit signed numbers using 2's complement representation system. Also indicate if overflow has occurred.

   (i) (-9) + (-7)

   (ii) (+7) - (-8)

3. Define exception and explain two of its kinds.

4. Give the control sequence for the execution of instruction ADD (R3), R1.

5. Define the following:

   (i) Memory latency

   (ii) Memory bandwidth

   (iii) Hit rate

   (iv) miss penalty

## SECTION D

Attempt **any two** questions from the following. Each question carries equal marks.

[2x10=20]

1. What is virtual memory? With a diagram, explain how virtual memory address is translated.

2. Let you have a 256 MB main memory, and a 1 MB cache memory. The address space of the c/oncerned processor is 256 MB. Block size is 128 bytes and there are 8 blocks in a cache set.

   With the aforementioned specification, determine the size of sub-fields ( in bits) in the address for direct mapping, associative and set associative mapping cache schemes.

3. Explain the parallel I/O interface with a block diagram.

## SECTION E

Write short notes on **any two** of the following. Each carries equal marks. [2x10=20]

1. Addressing modes
2. RISC
3. Cache Coherence

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