Paper Code & Roll No. to be filled in your Answer Book

Roll No. | | | | | | | | | | |

B.Tech. (IV - Sem.)

Even Semester Examination - 2016

COMPUTER ORGANIZATION

[Time : 3 Hours] *[Maximum Marks :100]*

Note: Attempt **all** questions, each questions carry **equal** marks

Q1. Attempt **any four** parts of the following: (5×4=20)

(a) Design an arithmetic circuit with one selection variable and two n-bit data inputs A & B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	C_{in}=0	C_{in}=1
0	D=A+B	D=A+1
1	D=A-1	D=A+B'+1

(b) Show the multiplication process using Booth algorithm when the following binary numbers are multiplied: (12)*(-15).

(c) Find the expression for generation of carry-in four bit carry-look ahead adder. Also draw its logic diagram.

(d) What do you mean by Bus transfer. Draw a diagram of bus system for four registers of 4-bits each. The bus is to be constructed with multiplexers.

(e) Represent decimal number -0.654 into IEEE floating point format.

(f) Design Arithmetic Logic Shift unit that will perform different arithmetic, logic and shift operation.

Q2. Attempt **any four** parts of the following: (5×4=20)

(a) Write the difference between hardwired and microprogrammed control unit.

(b) Write the sequence control step required for the structure of single bus organization for the of the following: **SUB (R3),R4**

Where R3 is source register and R4 is destination register.

(c) What do you mean by Bus organization? Explain multiple bus organization with block diagram.

(d) Explain micro program sequencer with the help of block diagram.

(e) What are the various phases for executing an instruction?

(f) Define control memory and microinstruction properly.

Q3. Attempt **any two** parts of the following: (10×2=20)

(a) Write a program to evaluate the arithmetic expression.

X= (A+B*C)/(D+E*F/G+H)

Using Zero and One address machine.

(b) Describe DMA with suitable block diagram. Why does DMA have priority over the CPU when both request a memory transfer? Explain.

(c) Explain the following with example:

(i) Direct addressing mode

(ii) Indirect addressing mode

(iii) Immediate addressing mode

(iv) Register indirect addressing mode

Q4. Attempt **any two** parts of the following: (10×2=20)

(a) Discuss various organization of RAM .A computer uses RAM chips of 1024*2 capacities. How many chips are needed and how should their address lines be connected to provide a memory capacity of 1024 bytes?

(b) Explain memory hierarchy in a computer system? A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with block size of four words. Find out the total numbers of bits in tag index, block and word fields of the address format.

(c) Discuss construction and working of a magnetic disk. Discuss various components of disk access time.

Q5. Attempt **any Two** parts of the following: (10×2=20)

(a) Draw a timing diagram for a six-stage pipeline showing how it would process eight tasks.

(b) Give various architectural classification schemes. Also discuss the Flyn,s and Feng,s classification in detail.

(c) Describe vector processor and array processor. Also explain their similarities and differences.