TCS /TIT- 401 40 Printed Pages : 6

Roll No. to be filled in your Answer Book

Roll No. | | | | | | | | | | | |

B. Tech. (Information Technology) (4TH Semester) Examination, 2015

Computer Organization

Time: 3.00 Hrs] **[Max. Marks: 100**

Note: All questions are compulsory.

Q1. Attempt any four parts: (5×4 = 20)

(a) What is shift micro operation? Explain logical shift, circular shift and arithmetic shift micro operation.

(b) Define bus arbitration. Also discuss serial bus arbitration with proper diagram.

(c) What do you mean by inter-register transfer? Discuss Bus transfer.

(d) Explain addition and subtraction algorithm with the help of flow chart.

(e) Multiply decimal –5 by decimal –6 using Booth's algorithm.

(f) Discuss IEEE standard for floating point numbe:

Q2. Attempt any four parts: (5×4 = 20)

(a) What do you mean by Control unit? Describe briefly a Hardwired control unit.

(b) Distinguish between a control memory and main memory used in a digital computer.

(c) What do you mean by the term Micro program Sequence? Explain the role played by it.

(d) Write short notes on the following:

(i) Microinstruction

(ii) Micro Program

(e) Explain wide-branch addressing and emultion.

(f) Explain:

(i) Fetching a word from memory

(ii) Storing a word in memory

Q3. Attempt any two parts: (10×2 = 20)

(a) Write the program to evaluate the arithmetic statement X = (A + B * C) / (D – E * F + G * H):

(i). Using a general-register-type computer with three-address instructions.

(ii) Using a general-register-type computer with two-address instructions.

(iii) Using an accumulator-type computer with one-address instructions.

(iv) Using a stack-organized computer with zero-address operation instructions.

(b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is :

(i) Direct

(ii) Immediate

(iii) Relative

(iv) Index with R1 as index register

(v) Register indirect

(c) (i) What is DMA scheme of data transfer? Discuss its operating principle.

(ii) What is an interrupt? Describe its significance for digital computers. Also discuss various types of interrupts in brief.

Q4. Attempt any two parts: (10×2 = 20)

(a) Explain the need of memory hierarchy with the help of a block diagram? What is the reason for not having one large memory unit for storing all information at one place?

(b) A digital computer has a memory unit of 64K × 16 and a cache memory of 1 K words. The cache uses direct mapping with a block size of four words.

(i) How many bits are there in the tag, index, block, and words fields of the address format?

(ii) How many bits are there in each word of cache, and how are they divided into functions?

(iii) How many blocks can the cache accommodate?

(c) Discuss the concept and implementation of virtual memory. Also describe a suitable scheme for translation from logical address to physical address.

5. Attempt any two parts: (10×2 = 20)

(a) A certain risc microprocessor has a five-stage pipeline operating according to the register-transfer specification given in the table supplied overleaf. The pipeline hardware detects all data hazard conditions and stalls the pipeline when necessary for correct program behaviour. You are asked to consider how such a pipeline would execute the following loop:

```
loop:  lw   $t0, ($s1)
       add  $s2, $s2, $t0
       sub  $s3, $s3, $t2
       add  $s4, $s4, $t2
       sw   $s4, ($s8)
       addi $s1, $s1, 4
       addi $s8, $s8, 4
```

```
slt  $t1, $t5, $s2
bne $t1, $0, loop
```

(i) Draw a space-time graph showing progression of the instructions for one itera of the loop through this pipeline.

(ii) How many cycles elapse between the initia of successive iterations?

(b) Explain the concept of pipelining, instruc pipelining, RISC pipelining and arithm pipelining.

(c) Write short notes on:

(i) Inter-processor Arbitration

(ii) Cache Coherence

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