TCE-303 1311

Odd Semester Examination 2018-19

B. Tech (CE) (SEMESTER-III)

BASIC SURVEYING

Time: 03:00 Hours **Max Marks :50**

Note: Attempt **ALL** questions.All Questions carry EQUAL marks.In case of numerical problems assume data whenever not provided.Don't write anything on the question paper except your roll no.

1. Attempt **any two**of the following: [2x5=10]

   (a) What is the first principle of surveying? Explain the kind of errors would occur if we don't follow the first principle. Differentiate between plane and geodetic surveying.

   (b) What is the difference between total station and electronic theodolite? A plot is in the form of a regular hexagon. If one of the lines of the hexagon is along the direction N 23° 56' E, find the bearings of the other lines of the figure.

   (c) (i) A plan drawn to a scale of 1:4000 was measured by a scale of 1:5000. Find the % error in the length and area measured.

   (ii) The eye of an observer is 7.5m above sea level and he was able to see a lighthouse 50m high just above the horizon Find the distance between the observer and the lighthouse.

2. Attempt **any two**of the following: [2x5=10]

   (a) A distance of 2000m was measured by a 30m chain. Later on, it was detected that the chain was 0.1 m too long. Another 500m (total 2500m) was measured

(d) Implement following Boolean function using 3:8 decoder and external gates.

$f(A,B,C)=\sum m(2,4,5,7)$

(e) Design 4:16 decoder using two 3:8 decoder.

(f) Write short notes on PAL and PLA.

3. Attempt **any two** questions from the following : [2x10=20]

(a) Draw and explain working of Edge triggered JK flipflop. Also explain how it differs with T flip flops.

(b) With a neat diagram explain operation of a 4 bit left shift register. Also draw its timing diagram.

(c) Convert JK flipflop into D and SR flipflop.

4. Attempt **any two** questions from the following : [2x10=20]

(a) Discuss in detail about TTL and ECL logic families.

(b) Describe following characteristics of logic families-

Fan out, Fan in, Figure of Merit, propagation delay and Noise Margin

(c) Implement below function using CMOS logic

$Y=\bar{A}+\bar{B}+C$

5. Attempt **any two** questions from the following : [2x10=20]

(a) What is meant by Hazard in a logic network? Discuss different types of Hazards.

(b) Draw circuit diagram of MOS static RAM cell. Also explain its working.

(c) (i) Write short note on DRAM. Explain its advantages and disadvantages.

(ii) How many 256*8 memory chips are required to obtain a 2048*8 memory?

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