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TEC 101	
Roll No.	
ODD SEMESTER EXAMINT	TION 2019-20
B. TECH (SEM I) OLD SYLLA	BUS BACK PAPER
FUNDAMENTAL OF ELECTRONIC	[Total Marks: 100]
[Time: 3 HOURS]	Total no. of printed pages: 2

Note: Attempt all the questions. All questions carry equal marks

Attempt any four parts of the following: 01.

(5*4=20)

- a) Differentiate between Donor impurities & Acceptor impurities. For converting intrinsic silicon into n-type material which type of impurities are added and which material is preferred as Donor and Acceptor.
- b) Define conductivity. Derive the expression of conductivity in intrinsic and extrinsic semiconductors.
- c) Describe how p-type and n-type semiconductors are produced. State the main difference
- d) Draw and explain V-I characteristics of p-n junction. Explain how Depletion layer develops in the diode.
- e) Draw the energy band diagram of intrinsic and extrinsic (n and p-type) semiconductors.
- f) At room temperature the reverse saturation current is 0.3μA when a reverse bias is applied to a germanium diode. Find the value of current flowing in a diode when 0.15V forward bias is applied.

Attempt any four parts of the following: Q2.

(5*4=20)

- a) Explain Voltage Doubler and Tripler circuits.
- b) Draw the circuit diagram of full wave rectifier using two diodes and explain its working showing input and output waveforms. Derive I_{dc} , I_{rms} and PIV for the same.
- c) Derive the expression of ripple factor and efficiency of Bridge rectifier.

- e) The turns ratio of a transformer used in a half wave rectifier is n1: n2 = 12:1. The primary is connected to power mains 220V, 50 Hz. Assuming the diode resistance in forward bias to be zero, calculate the dc voltage across the load. What is the PIV of the diode?
- f) Explain the application of zener diode as a shunt regulator

Attempt any TWO parts of the following: Q3.

(10*2=20)

- a) Draw and explain the i/p & o/p characteristics of BJT in CE configuration, indicating the operating regions. Also explain why CE configuration is most widely used in amplifier circuits.
- b) Define with respect to BJT the following ICEO. ICBO, α,β , STABILITY FACTOR.
- c) Derive the hybrid parameters expression for Ai, Ri, Av and Ro for CE amplifier.

P.T.O

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Q4. Attempt any TWO parts of the following:

(10*2=20)

- a) Explain the construction and working of the n channel JFET. Also draw the drain and transfer characteristics.
- b) Distinguish E-MOSFET and D-MOSFET. Also explain the working of p-channel E-MOSFET.
- c) Derive the expressions for Voltage Gain, Input resistance, Output Resistance for common source n channel JFET amplifier with Fixed bias.

Q5. Attempt any TWO parts of the following:

(10*2=20)

- a) Minimize the following using K Map $F(a,b,c,d) = \sum_{m} (3,4,5,7,9,13,14,15) + \sum_{m} d(0,1,8,10)$
- b) Design AND, OR, NOR GATE USING NAND gate.
- c) Derive the close loop voltage gain expression (A_f) of Inverting and Non
 - i. Non-Inverting Amplifier.
 - ii. Draw the circuit diagram and explain Multiplier using OP AMP.