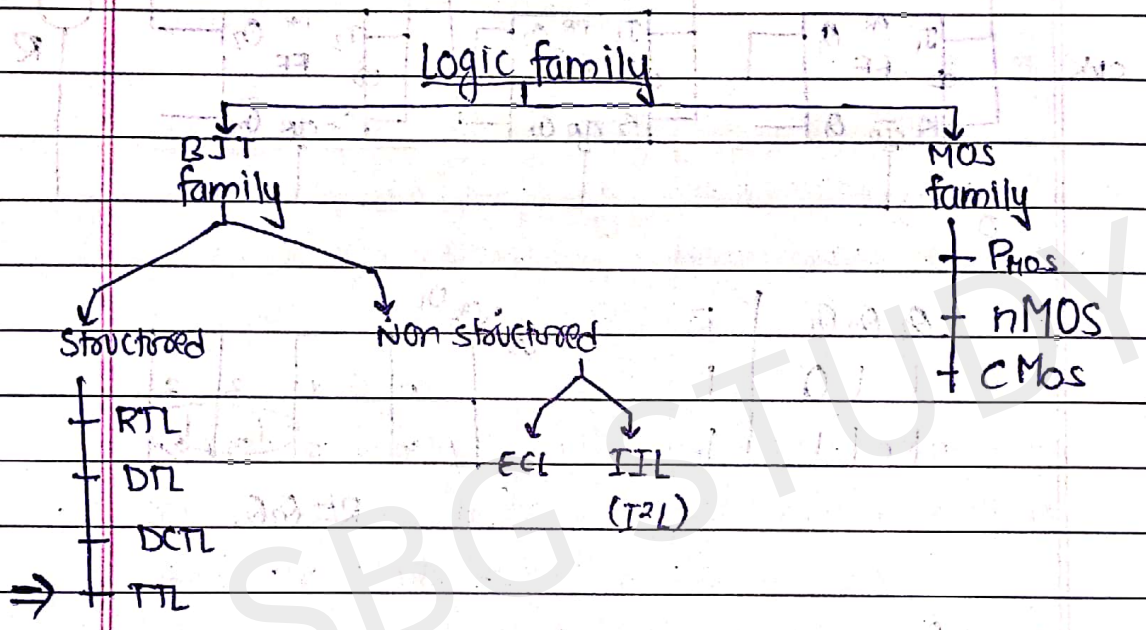
Ramwar.

UNIT-4

Date: / /

LOGIC FAMILIES:

logic family is nothing but the collection of devices having similar operating characteristic. logic families are realised by using same type of semiconductor device. Depending upon the type of semi conductor device used logic families are classified as.



RTL : register transistor logic
DTL : Diode " "
DCTL : Diode coupled " "
TTL : Transistor " "
ECL : emitter coupled logic
IIL : integrated injection logic.
PMOS : P-channel metal oxide semiconductor
nMOS : n " " " "
CMOS : complementary " " "

Date: / /

Performance parameters of logic families

The performance of a logic family is governed by following parameters:

(1) Propogation Delay
(2) Power Dissipation
(3) noise immunity/noise margin
(4) fan-in
(5) fan-out
(6) operating temperature
(7) voltage parameters.

- **Propogation Delay**

it is defined as time taken by output to change after the input has changed. it is the measure of speed of operation. Higher the propogation delay slower will be the device and vice-versa.

Each logic family encounters two type of propogation delays t_{PHL} and t_{PLH}.

t_{PHL} is the propogation delay time taken by the output to change from logic High (1) to logic low (0).

t_{PLH} is the propogation delay time taken by the output to change from logic low to logic High

The average propogation Delay can be calculated by the relation

$$= \frac{t_{PHL} + t_{PLH}}{2}$$

Date: / /

- **Power Dissipation (PD)**
  it is the measure of the power consumed by the logic gate when driven by all its inputs. smaller the PD better will be the device. PD is the product D.C. supply voltage and the mean current drawn from the supply.

  $$P = V_{cc} \times I$$

- **Noise immunity**
  noise is a unwanted signal that tends to affect the performance of the logic circuit. Noise can cause the output to fall below logic low level or rise above the logic high level.
  Noise immunity is the max. noise voltage that may appear at the input of the logic circuit without changing its output state.
  Noise margin is the quantitative measure of noise immunity.

- **Fan-in**
  it is defined as the max. no. of input that can be connected to the logic circuit without any degradation in its performance. it can also be defined as the no. of inputs that the device is designed to handle.

Date: / /

- **Fan-out:**

it is defined as the no. of gates that can be driven by the single output of a logic family. The deriving gate must be capable of providing the voltage & current & level required by the driven gates. This can be acheived by having low output impedence.

- **Operating temperature**

it is the max. " in which the device can with stand

- **Voltage parameters :-**

V_{IL} (min)
V_{IL} (max)
V_{OH} (min)
V_{OH} (max)

V_{IL} (Min): it is the min. voltage level required at the input of the gate so that the input can be treated as logic 1.
its minimum value is 2 volt.

V_{IL} (max): it is the max. value of the input voltage. so that the input can be treated as logic 0.
The maximum value is 0.7 volt

V_{OH} (min): it is the high level output voltage and can be defined as the min. voltage level required at the o/p so that the o/p can be treated as logic 1.
its min. value is 2.4 volt.

$\overline{=}$ > logic '0'

V_{cc} < logic '1'

Date: / /

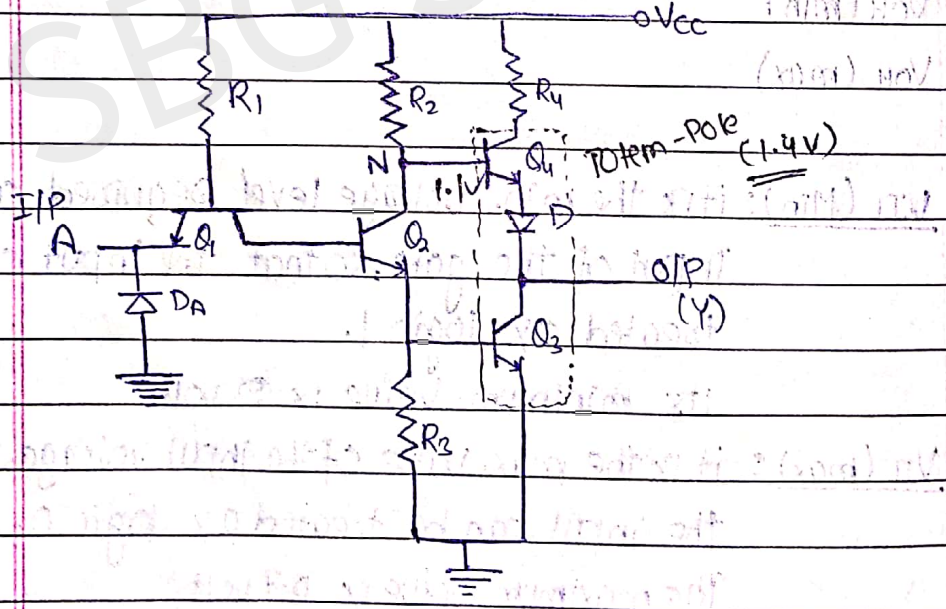
$V_{OL(max)}$: it is defined as the max. voltage level required at the output so that the output can be treated as logic 0.
Its max. value is 0.4 Volt.

10 marks Imp. ⇓

TTL (Transistor transistor logic)

it uses transistors for both the inputs and the outputs and that is why named as transistor transistor logic. it is used to realise the function of various logic gates.

TTL inverter



I/Ps	Transistors				O/P
A	Q_1	Q_2	Q_3	Q_4	Y
1	ON	ON	ON	OFF	0
0	ON	OFF	OFF	ON	1

Date: / /

Working :-

The Base of transistor Q_1 is always connected to the supply (V_{cc}) and therefore it will always be ON.

case I: When input A = 0.

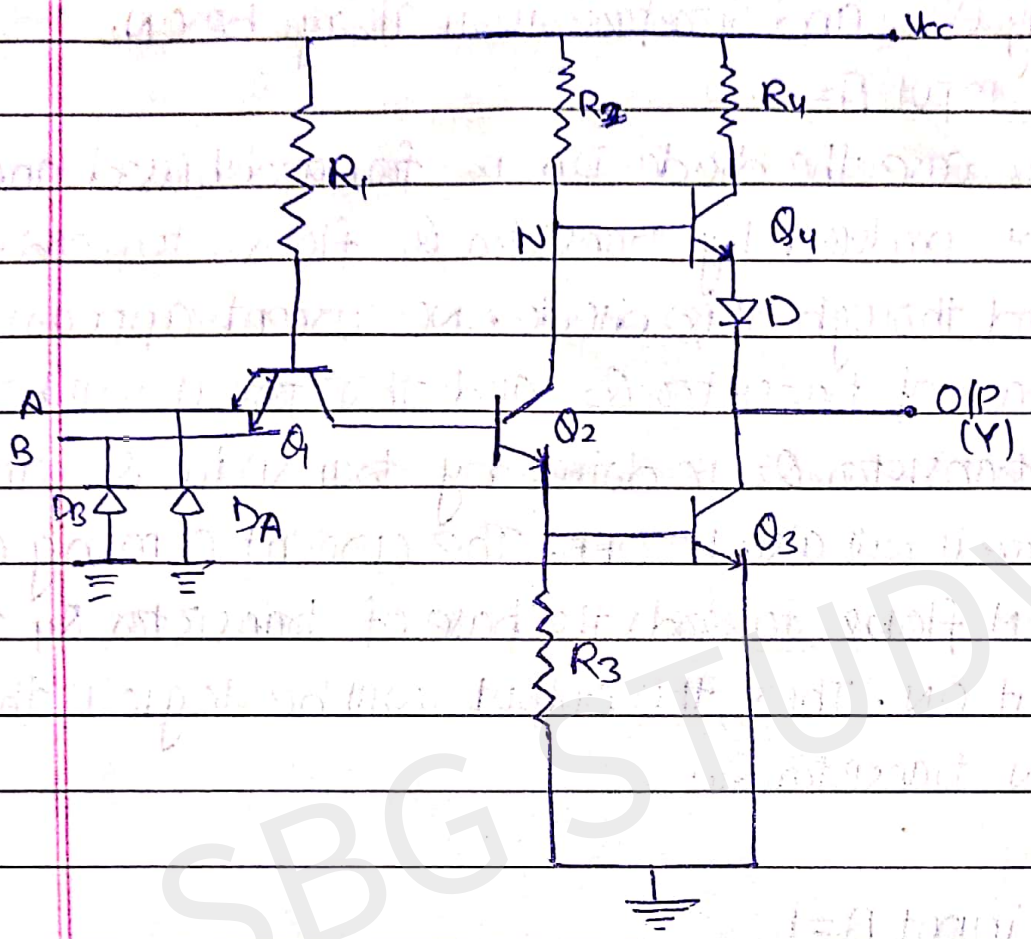
in this case the diode D_A is forward biased and current produced by transistor Q_1 flows, towards ground through this diode. NO current appears at the base of transistor Q_2 and therefore it will be OFF. Since transistor Q_3 is driven by transistor Q_2 and therefore it will also be OFF. The current coming at the node N flows towards the base of transistor Q_4 and turns it ON. Thus, the output will be logic '1' through the ON transistor Q_4.

case II: When input A = 1

in this case diode D_A is reversed biased and it acts as an open circuit. The current produced by transistor Q_1 flows towards the base of the transistor Q_2 and turns it ON. Since transistor Q_3 is driven by Q_2 therefore it will also be ON. current coming at node N flows towards ground through the ON transistor Q_2 and no current appears at the base of transistor Q_4 therefore it will be OFF. The output will be logic '0' through ON transistor Q_3.

Date: / /

TTL NAND gate:-



A	B	Q1	Q2	Q3	Q4	Y
0	0	ON	OFF	OFF	ON	1
0	1	ON	OFF	OFF	ON	1
1	0	ON	OFF	OFF	ON	1
→ 1	1	ON	ON	ON	OFF	0

Date: / /

Working:-

The Base of the transistor Q_1 is always connected to the supply (V_{cc}) and therefore it will be always ON.

Case I: when any of the input is 0

in this case the corresponding diode will be froword biased and the current produced by Q_1 will flow towards ground through that diode. NO current

Case II: when both input are logic 1.

in this case none of the diode D_A and D_B will be froword biased and both will act as open circuit. The current produced by transistor Q_1.

Ques para h

Date: / /

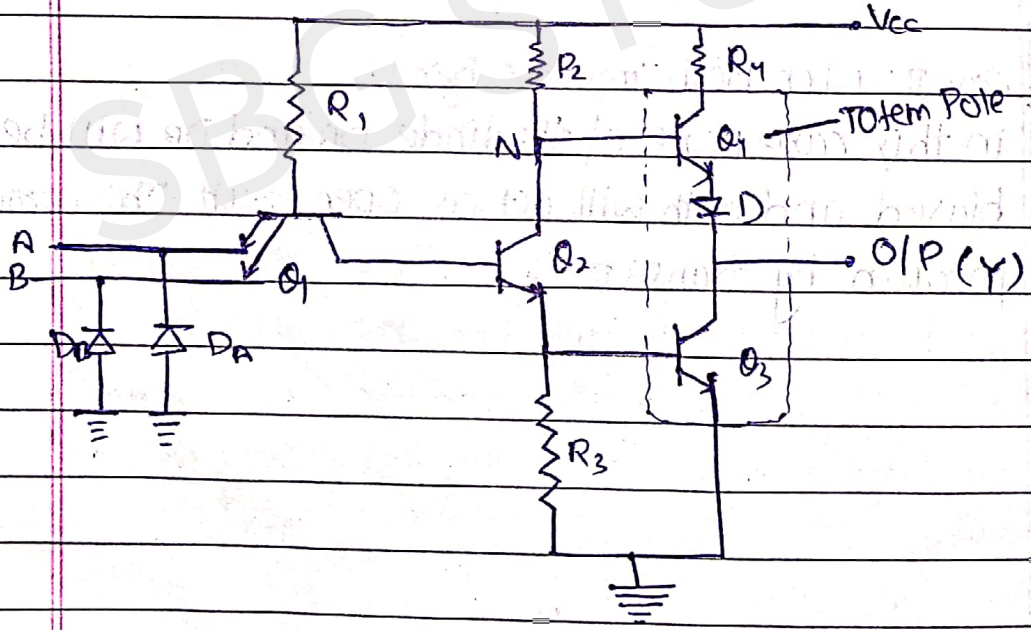
TTL Output configuration :-

The output of TTL gate can be connected in any of the following three ways :-

(i) Totem-Pole
(ii) Open-collector
(iii) Tristate / High impedance

Totem-pole configuration :-

TTL NAND gate in totem pole output configuration can be ~~shown~~ drawn as shown:



This configuration is specifically designed to reduce propogation delay of the circuit, in this ~~to~~ two transistors are sit above each other with the diode in between them and ∴ named as totem pole.

Date: / /

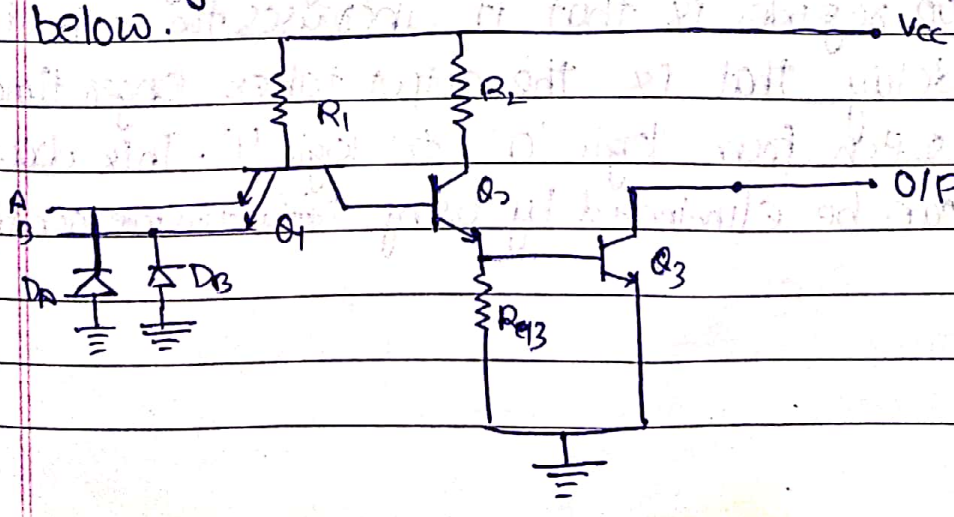
The output of this configuration is obtained as high voltage or logic '1' when transistor Q_4 is ON and as low voltage as logic '0' when transistor Q_3 is ON. The circuit is designed in such a way that both Q_3 and Q_4 can never be ON at the same time. This is achieved by having a diode in between Q_3 and Q_4. For Q_3 and Q_4 to be ON at the same time the min. voltage required at the base of Q_4 is 1.4 volt but, after voltage calculations, the available voltage at the base of Q_4 is 1.1 volt. Therefore Q_3 and Q_4 cannot be ON at the same time.

Draw back of totem Pole

The draw back of totem pole configuration is that when either Q_3 ~~and~~ or Q_4 conducts the output impedence becomes very low and it causes serious loading problem. This problem can be eliminated by using open collector configuration.

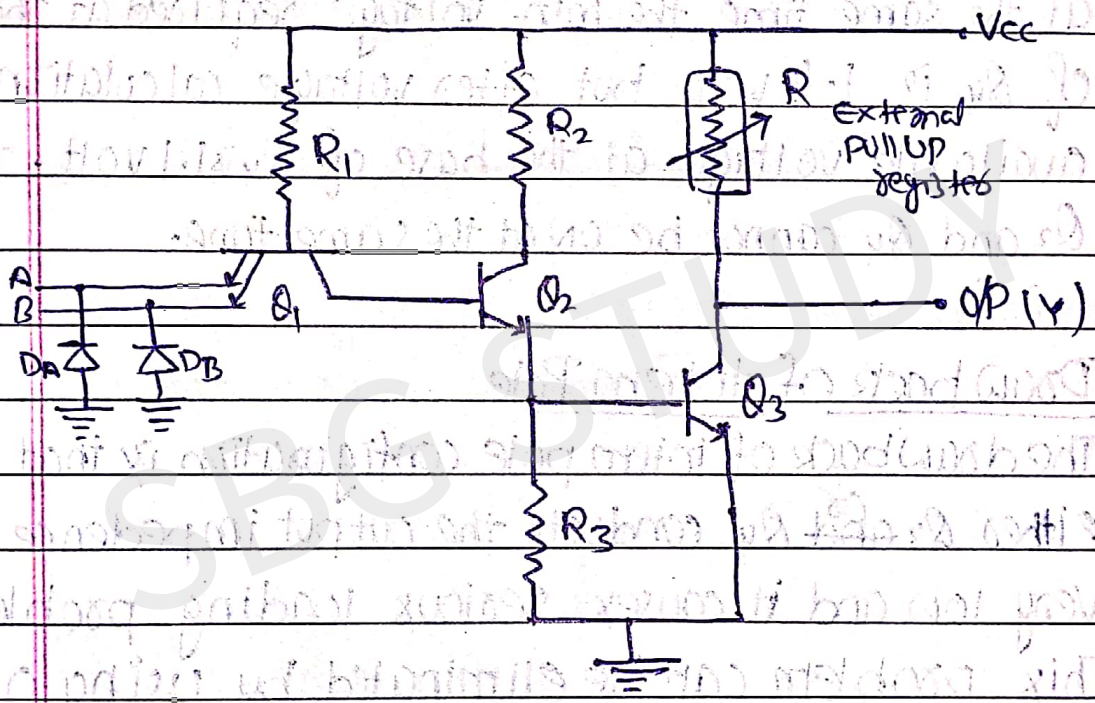
Open collector configuration

The open collector configuration is obtained by opening the collector of transistor Q_3 as shown below.



Date: / /

This configuration produces two states. low voltage or logic '0' when Q_3 is ON and high impedance state. The main problem of open collector configuration is that it doesnot have the logic '1' state. This problem can be eliminated by using an external pull up register as shown below:



The external pull up register takes output from logic '0' to logic '1' and is connected between pull down ~~reg~~ transistor and supply.

The dis advantage of connecting a ~~high~~ large external pull up register is that it increases the switching delay that is the output takes longer time to switch from logic '0' to logic '1'. This drawback can be eliminated by using ~~this~~ tristate configuration

Date: / /

Tristate configuration