HAZARDS

After designing a combinational circuit, it is required to ensure that the designed circuit is free of operating errors. There are chances that the O/P may be in error due to noise or malfunctioning of the circuit for a temporary period.

This malfunction of the logic circuits is defined as hazards.

In combinational circuits, hazards result in false O/P value. Hazard is a condition where a single variable change produces a momentary O/P change, when no O/P change should occur. Hazards may be divided in 2 categories:

Static Hazard and Dynamic Hazard:

1. Static Hazard → May be defined as a transient change of an O/P value which is supposed to remain fixed during the transition of value of a single variable.

Static hazards are further divided into:

Static '0' & Static '1'

Static '0' when O/P is supposed to remain at '0' but it is likely to go to '1', momentarily during transition of I/P then hazard is then static '0'.

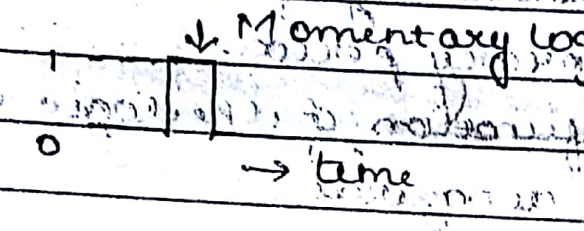
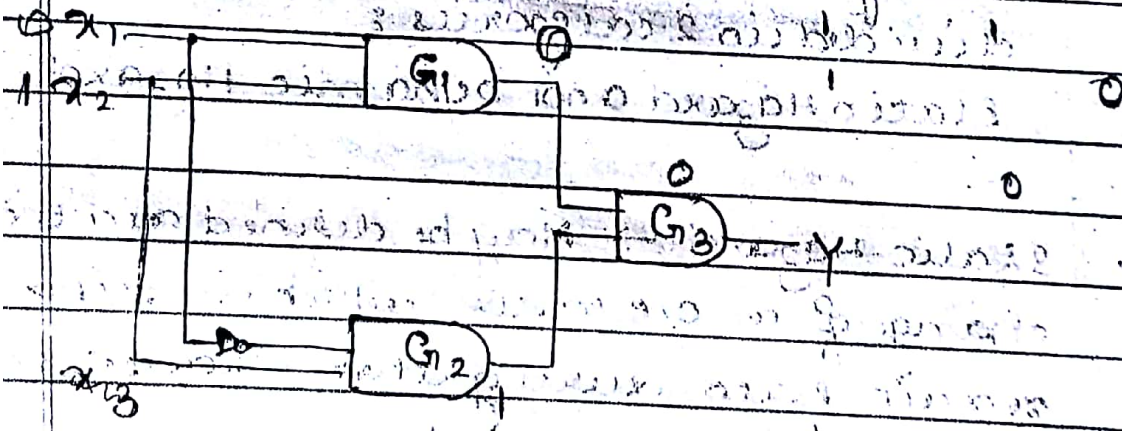


Illustration of logic '0' hazard :-

In order to illustrate occurence of static '0', consider following combinational ckt.



eg. if $x_1 = 0$ & $x_2 = 1$, $Y = 0$

$x_1 = 1$, $x_2 = 1$, $Y = 0$

O/P is fixed but due to NOT gate there could be delay, corresponding to which we get $Y = 1$. So, there is hazard.

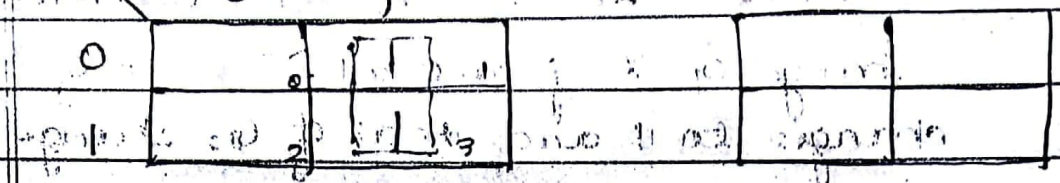
Assume that $x_1 = 0$ and $x_2 = 1$. This causes the O/P of G_1 to be 0, that of G_2 would be 1 and $\therefore G_3 = Y = 0$. Now, consider a change of x_1 from 0 to 1. The O/P of Gate 1 changes to 1 and that of G_2 changes to 0. However, the O/P may momentary go to logic '1', if the propagation delay through inverter is taken into consideration. This delay may cause the O/P of G_1 to change to 1, before the O/P of G_2 changes to 0. In that case, both I/Ps of G_3 are momentarily equal to 1, causing the O/P to go to 1 for this short interval of time.

Elimination of static '0' hazard :-
The static '0' hazard can be eliminated using following steps,

1. Obtain boolean expression of given circuit.
2. Obtain k-map for the boolean expression.
3. Find redundant pair and quad.
4. Draw the new k-map to make circuit hazard free.
5. Write boolean expression that includes all possible combinations of k-map.
6. Redesign the circuit to obtain hazard free circuit.

$Y = (x_1 + x_2)(x_1' + x_2)$.

By K-map.



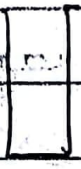
$Y = x_2$

There are no redundant pair or quad.

Therefore, the simplified $Y = x_2$.

Static '1' hazard

When O/P is supposed to remain at 1, but it is likely to go to logic '0' momentarily during transition of I/P state, hazard is called static '1' hazard.



→ time

↑ momentary logic '0' O/P

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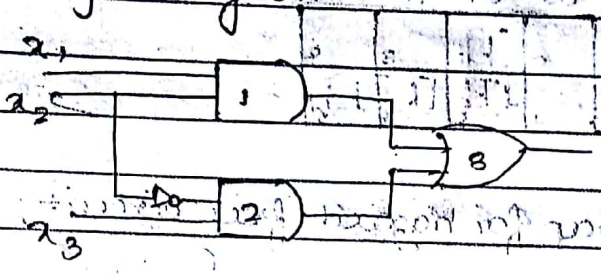
Illustration :- In order to illustrate the occurence of static '1', consider the following logic diagram.

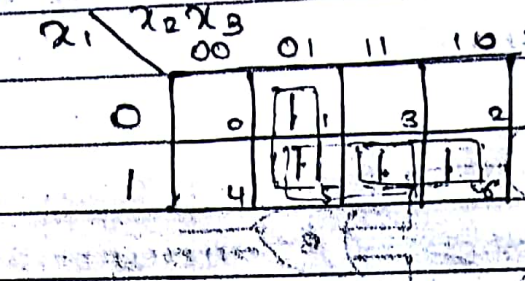


Assume that all the three I/Ps are equal to 1 initially. This causes the O/P of gate 1 to be 1, that of gate 2 to be 0 and O/P of the circuit to be equal to 1. Now, consider a change of x_2 from $1 \to 0$. The O/P of G_1 changes to 0 and that of G_2 changes to 1. However, the O/P of ckt may momentarily go to 0 if propagation delay through the inverter is taken into consideration. This delay may cause the O/P of G_1 to change to 0 before O/P of G_2 changes to 1. In that case, both I/Ps of G_3 are momentarily equal to 0, causing the O/P to go to 0 for a short time interval.

Elimination of "static 1" hazard :-

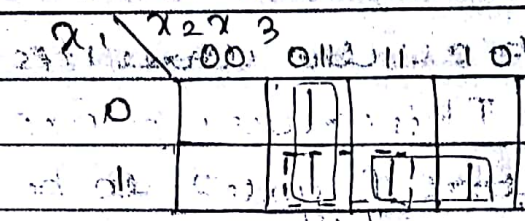
$$Y = x_1x_2 + \bar{x}_2x_3$$

The K-map for the above;



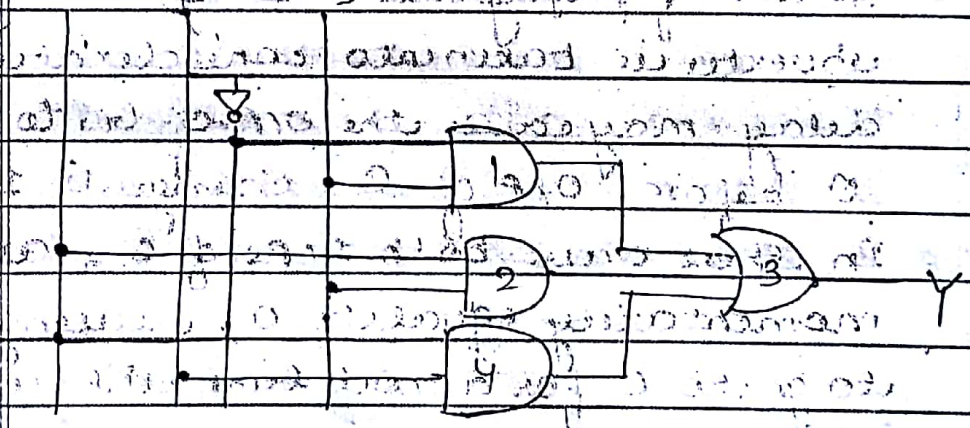
New K-map for hazard free circuit;

finding possible combination



↳ New pair to eliminate static '1' hazard

$Y = \bar{x}_2 x_3 + x_1 x_3 + x_1 x_2$

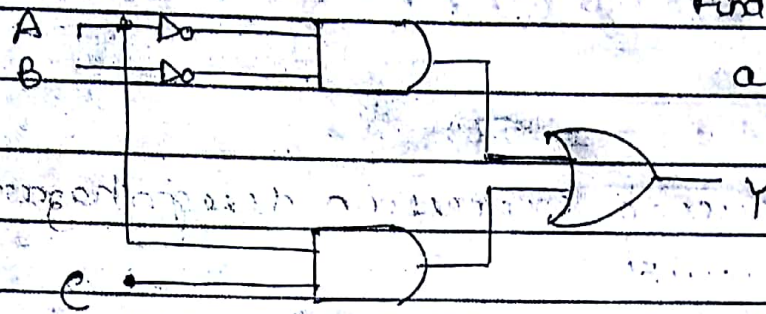


Gate 4's value is independent of value of x_2, so hazard is removed.

changing x_2 from 1 → 0 would affect o/p of G4 and hence, o/p will remain 1 even if delay through inverter is taken into account

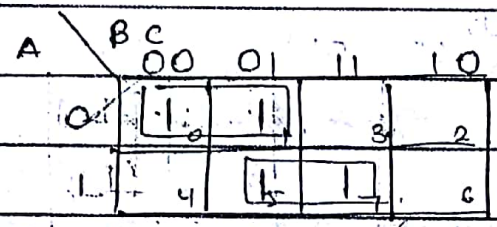
Q. Modify the circuit to make it hazard free.

Find type of hazard and then ; ... (above).

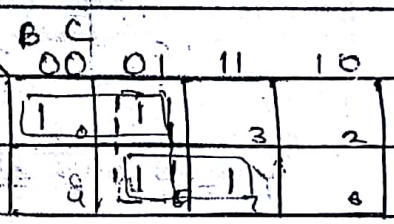


Ans

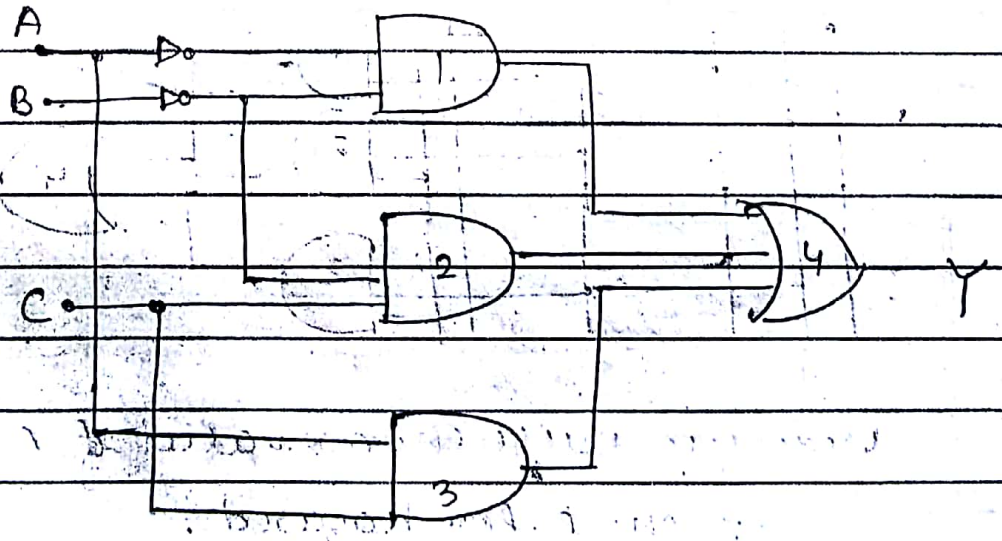
$$Y = \bar{A}\,\bar{B} + AC$$



New K-map,



$$Y = \bar{A}\,\bar{B} + \bar{B}C + AC$$



we will vary value of A and then find out which hazard lie there.

Here, initial value of A, B, C would 0 0 1.
(ĀBC)

Q. For following expression, design hazard free circuit,

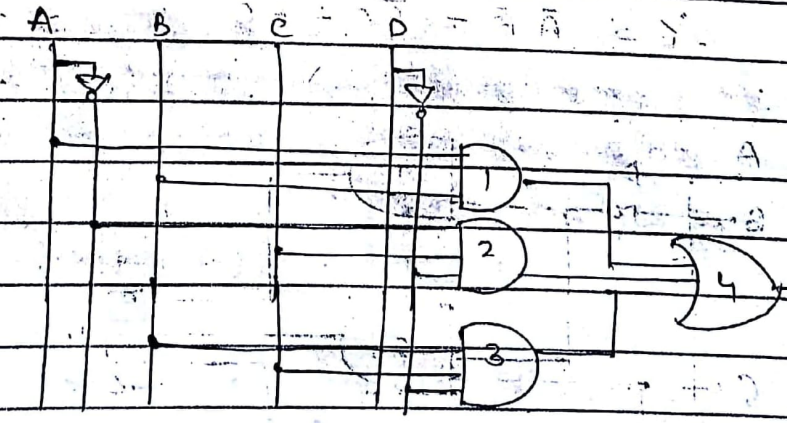
$$Y = AB + \bar{A}C\bar{D}$$

Soln:

$Y = AB + \bar{A}C\bar{D}$

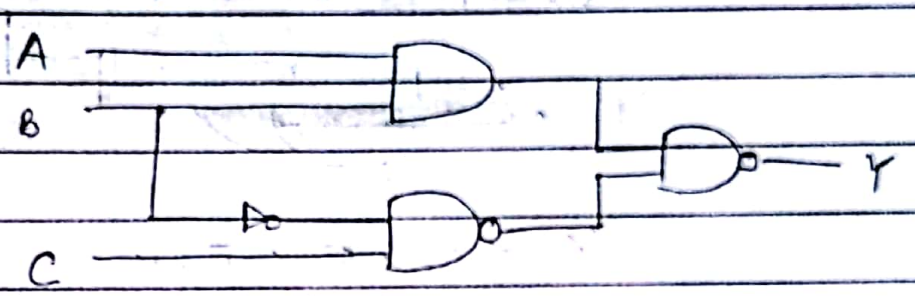
AB \ CD	00	01	11	10
00		1	3	1 2
01	4	5	7	1 6
11	1 12	1 13	1 15	1 14
10	8	9	11	10

$$Y = AB + \bar{A}C\bar{D} + BC\bar{D}$$



Here we will change value of A & then check for hazard.

Q. Show that a static hazard occurs for the circuit shown in fig. when I/P 'B' is changed from 0 to 1. Assume that the initial I/P state to be 101 i.e. A=1, B=0, C=1.



$$Y = \overline{(AB) + (\bar{B}C)}$$

$$Y = (\bar{A}\bar{B}) \cdot (\bar{B}C)$$

K-map.

A \ BC	00	01	11	10
0	1 (0)	1 (1)	3	2
1	4	1 (5)	7	6

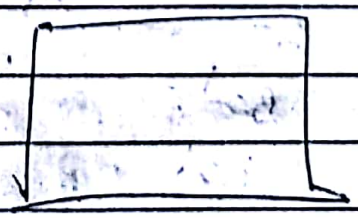
$$\overline{(AB) \cdot (\bar{B}C)}$$

$$(\bar{A}\bar{B}) + (\bar{B}C)$$

$$(\bar{A}\bar{B}) + (\bar{B}C)$$

01

0



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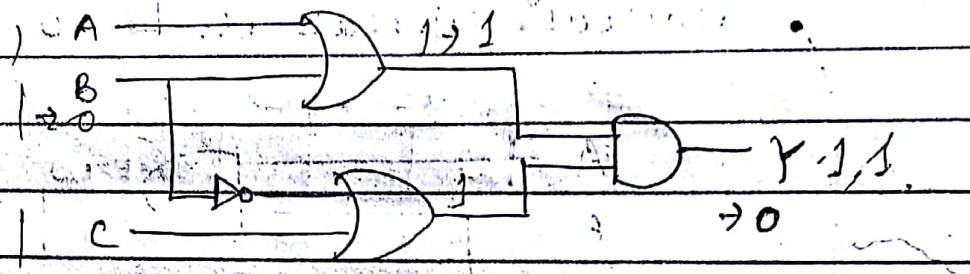
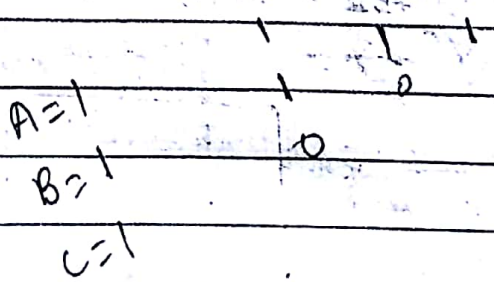
Q. Use K-map to detect static '0' hazard if any, for the following circuit.



$Y = (A + B)(\bar{B} + C)$

A \ BC	00	01	11	10
0	0 0	0 1	1 3	0 2
1	1 4	1 5	1 7	0 6

There is a redundant pair, it implies that hazard exists in the given circuit. From the ~~circuit~~ K-map it is clear that, if we change the value of B from 1 to 0 then the hazard occurs.



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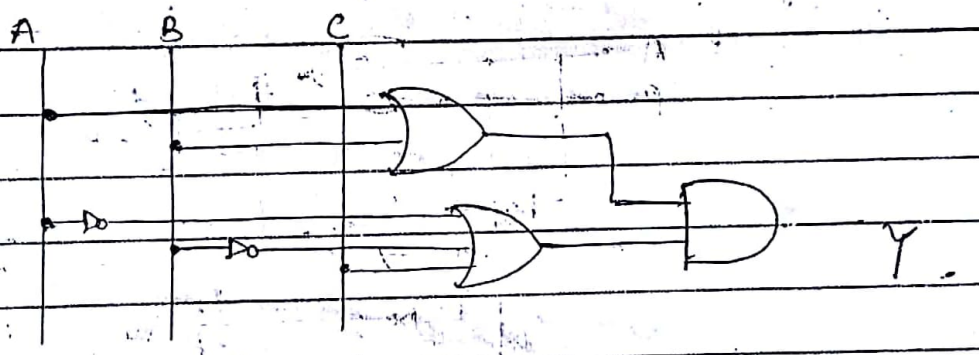
Maxterms = $(\bar{A} + \bar{B} + \bar{C})(\bar{A} + \bar{B} + \bar{C})$
$(\bar{A} + \bar{B} + C)$

A \ BC	00	01	11	10
0	0 (0)	0 (1)	3	2
1	4	5	7	0 (6)

$Y = \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} \cdot (A + B)(\bar{A} + \bar{B} + C)$



Q. $f = \bar{B}\bar{C} + \bar{A}C + AB$

Ans:- $f = \bar{B}\cdot\bar{C}(A + \bar{A}) + \bar{A}C(B + \bar{B}) + AB(C + \bar{C})$

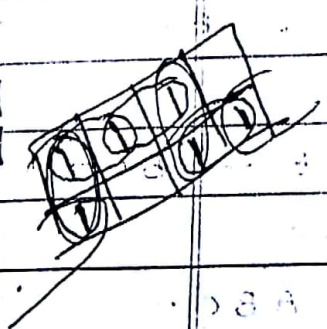
$= A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}C + ABC + AB\bar{C}$

$= A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC + AB\bar{C}$

100 000 011 111 110

4 1 3 7 6

A \ BC	00	01	11	10
0	1 (0)	1 (1)	1 (3)	1 (2)
1	1 (4)	5	1 (7)	1 (6)

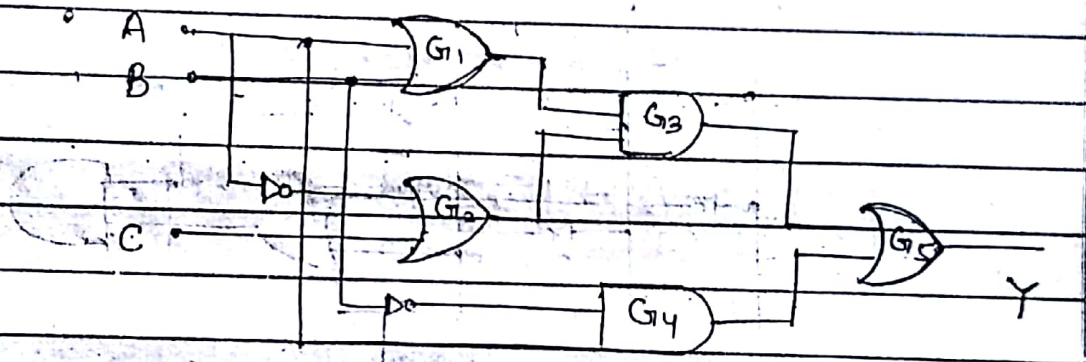


DYNAMIC HAZARDS :-

They occur when O/P of the circuit is to change from 1 logic level to the other logic level. But a momentary false O/P occurs during transition.

In dynamic hazards, the false O/P state occurs 3 or more than 3 times.

eg. consider the following circuit;



$Y = [(A+B)(\bar{A}+C)] + [(\bar{B}A)]$

$= A\bar{A} + AC + \bar{A}B + BC + A\bar{B} = AC + \bar{A}B + BC + A\bar{B}$

A \ BC	00	01	11	10
0	0	1	1	
1	1	1	1	

$Y = A\bar{B} + \bar{A}B + BC + AC$

$= A\bar{B}(C+\bar{C}) + \bar{A}BC(C+\bar{C}) + (A+\bar{A})BC + AC(B+\bar{B})$

$= A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + ABC + \bar{A}BC + ABC + A\bar{B}C$

$= A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + ABC$

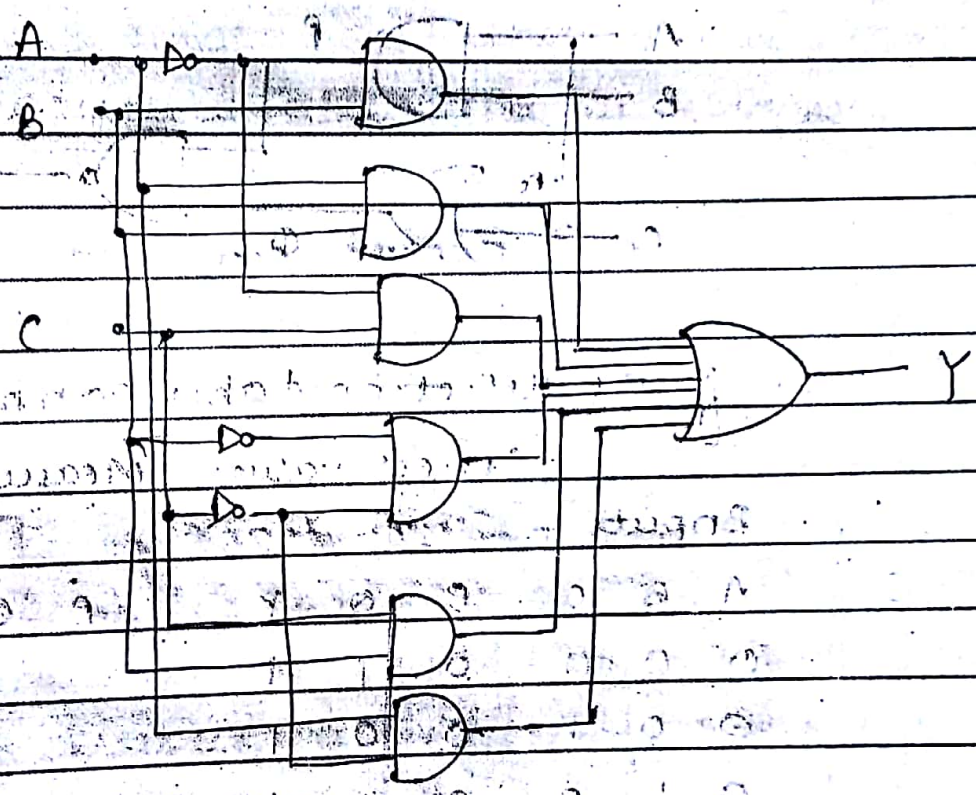
101 100 011 010 111

D → SOP

D → POS

Above circuit has dynamic hazards and there can be 3 more pairs.

$Y = \bar{B}\bar{C} + \bar{A}C + AB + \bar{A}B + BC + A\bar{C}$



fault detection :-

In fault detection, the aim is to find faulty component which causes mal-functioning of the circuit. In this, a fault table is used. A fault table is a table in which there is a row for every possible I/P combination and a column for every fault.

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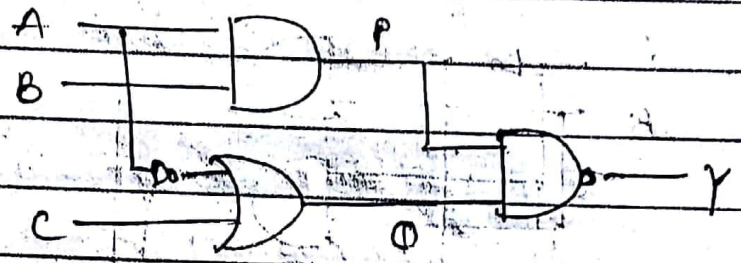
The fault detection is experimental analysis of combinational circuits.
eg. consider the following combinational circuit;



Now, fault detection table can be;

Inputs			Correct values			Measured values		
A	B	C	P	Q	Y	P	Q	Y
0	0	0	0	1	1			
0	0	1	0	0	1			
0	1	0	0	1	1			
0	1	1	0	0	1			

In case of ckt, instead of Y being 1 when A, B, C = 1 and if P = 0 and Q = 1 then it can be concluded that NAND Gate is faulty.

For each combination of I/Ps, the O/Ps available at P, Q and Y are measured and the measured values are recorded. These recorded values are compared with the correct values obtained by analysis of the circuit. If there is a difference b/w observed value and correct value, the stage at which error has occured can be determined and the faulty component can be located.

PATH SENSITISING METHOD:-

The PS M is used to detect and correct faults in combinational circuit. In this method, one variable is selected & its value is changed. The changes in O/Ps of gates can be traced down the line. Then the observed values and correct values are compared. By locating the place, where the error occurs, the faulty component can be traced and replaced.