SINGLE CORRECT TYPE QUESTIONS

1. An electric field is applied to a semi-conductor. Let the number of charge carriers be n and the average drift speed be v. If the temperature is increased
(A) Both n and v will increase
(B) n will increase but v will decrease
(C) v will increase but n will decrease
(D) Both n and v will decrease

2. The manifestation of band structure in solids is due to - **[AIEEE-2004]**
(A) Bohr's correspondence principle
(B) Pauli's exclusion principle
(C) Heisenberg's uncertainty principle
(D) Boltzmann's law

3. P-type semiconductor is formed when
A. As impurity is mixed in Si
B. Al impurity is mixed in Si
C. B impurity is mixed in Ge
D. P impurity is mixed in Ge
(A) A and C (B) A and D (C) B and C (D) B and D

4. In extrinsic semiconductors -
(A) The conduction band and valence band overlap
(B) The gap between conduction band and valence band is more than 16 eV
(C) The gap between conduction band and valence band is near about 1 eV
(D) The gap between conduction band and valence band will be 100 eV and more

5. A strip of copper and another of germanium are cooled from room temperature to 80 K. The resistance of - **[AIEEE-2004]**
(A) copper strip increases and that of germanium decreases
(B) copper strip decreases and that of germanium increases
(C) each of these increases
(D) each of these decreases

6. In a semiconductor, the concentrations of electrons and holes are $8 \times 10^{18}/m^3$ and $5 \times 10^{18}/m^3$ respectively. If the mobilities of electron and hole are 2.3 m^2/ volt-sec and 0.01 m^2/volt-sec respectively, then semiconductor is
(A) N-type and its resistivity is 0.34 ohm-metre
(B) P-type and its resistivity is 0.034 ohm-metre
(C) N-type and its resistivity is 0.034 ohm-metre
(D) P-type and its resistivity is 3.40 ohm-metre

7. No bias is applied to a P-N junction, then the current -
(A) Is zero because the number of charge carriers flowing on both sides is same
(B) Is zero because the charge carriers do not move ?
(C) Is non-zero
(D) None of these

8. You have three identical pn junctions; junction 1 is unbiased, junction 2 is reverse biased and junction 3 is forward biased. From largest to smallest, rank the three junctions according to the magnitude of their diffusion currents,

(A) 1,2,3 (B) 3,1,2 (C) 3, 2,1 (D) 2,3,1

9. In an unbiased n-p junction electrons diffuse from n - region to p - region because :

(JEE-Main Online-2015)

(A) Holes in p - region attract them

(B) Electrons travel across the junction due to potential difference

(C) Only electrons move from n to p region and not the vice - versa

(D) Electron concentration in n - region is more as compared to that in p - region

10. In a p-n junction diode -

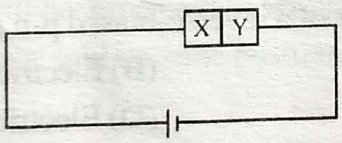
(A) new holes and conduction electrons are produced continuously throughout the material

(B) new holes and conduction electrons are produced continuously throughout the material except in the depletion region

(C) holes and conduction electrons recombine continuously throughout the material '

(D) holes and conduction electrons recombine continuously throughout the material except in the depletion region

11. A semiconductor X is made by doping a germanium crystal with arsenic (Z = 33). A second semiconductor Y is made by doping germanium with indium (Z = 49). The two are joined end to end and connected to a battery as shown. Which of the following statement is correct -



(A) X is P-type, Y is N-type and the junction is forward biased

(B) X is N-type, Y is P-type and the junction is forward biased

(C) X is P-type, Y is N-type and the junction is reverse biased

(D) X is N-type, Y is P-type and the junction is reverse biased

12. In a P-N junction diode not connected to any circuit -

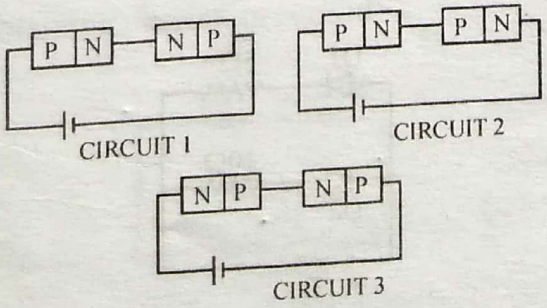
(A) the potential in the same everywhere

(B) the P-type side is at a higher potential then the N-type side

(C) there is an electric field at the junction directed from the N-type side to the P-type side

(D) there is an electric field at the junction directed from the P-type to the N-type side

13. Two identical p-n junction may be connected in series with a battery in three ways as shown in the adjoining figure. The potential drop across the p-n junction are equal in



(A) Circuit 1 and circuit 2 (B) Circuit 2 and circuit 3

(C) Circuit 3 and circuit 1 (D) Circuit 1 only

14. A semiconductor device is connected in a series circuit with a battery and a resistance. A current is found to pass through the circuit. If the polarity of the battery is reversed, the current drops almost to zero. The device may be -

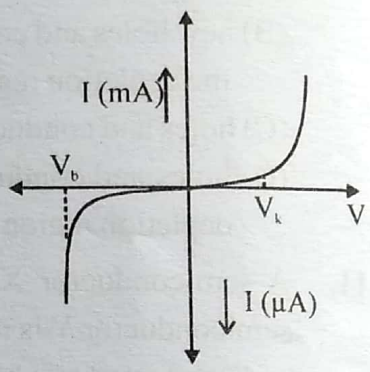
(A) A P-type semiconductor
(B) An N-type semiconductor
(C) A P-N junction
(D) An intrinstic semiconductor

15. When p-n junction diode is forward biased, then. **[AIEEE-2004]**

(A) both the depletion region and barrier height are reduced
(B) the depletion region is widened and barrier height is reduced
(C) the depletion region is reduced and barrier height is increased
(D) both the depletion region and barrier height are increased

16. The V-I characteristic for a p-n junction diode is plotted as shown in the figure. From the plot we can conclude that

V_b → breakdown voltage, V_k → knee voltage]

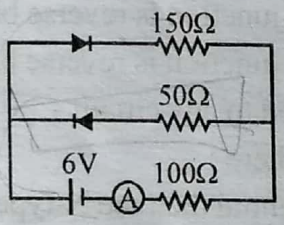


(A) the forward bias resistance of diode is very high; almost infinity for small values of V and after a certain value it becomes very low
(B) the reverse bias resistance of diode is very high in the beginning upto breakdown voltage is not achieved
(C) both forward and reverse bias resistances are same for all voltages
(D) both (A) and (B) are correct

17. In the middle of the depletion layer of a reverse-biased p-n junction, the :-

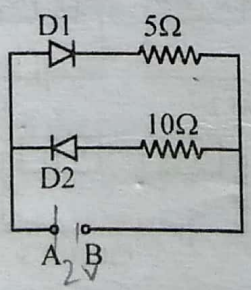
(A) Potential is maximum
(B) Electric field is maximum
(C) Potential is zero
(D) Electric field is zero

18. In the below given arrangement determine the ammeter reading, if each diodes have a forward resistance of 50 Ω and infinite backward resistance -



(A) zero
(B) 0.02
(C) 0.03
(D) 0.036

19. A 2V battery is connected across AB as shown in the figure. The value of the current supplied by the battery when in one case battery's positive terminal is connected to A and in other case when positive terminal of battery is connected to B will respectively be :- **(JEE-Main Online-2015)**



(A) 0.1 A and 0.2 A
(B) 0.4 A and 0.2 A
(C) 0.2 A and 0.4 A
(D) 0.2 A and 0.1 A

20. The dominant mechanisms for motion of charge carriers in forward and reverse biased silicon P-N junctions are -

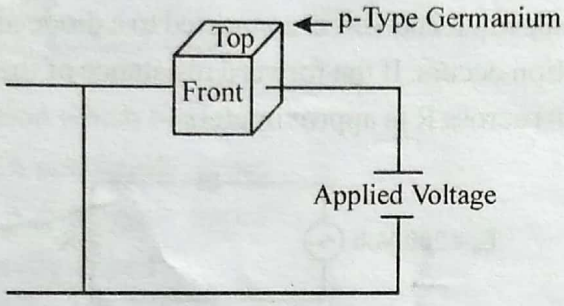
(A) Drift in forward bias, diffusion in reversebias

(B) Diffusion in forward bias, drift inreversebias

(C) Diffusion in both forward and reverse bias

(D) Drift in both forward and reverse bias

21. A cube of germanium is placed between the poles of a magnet and a voltage is applied across opposite faces of the cube as shown in Figure. Magnetic field is directed vertical downward in the plane of the. paper. What effect will occur at the surface of the cube?



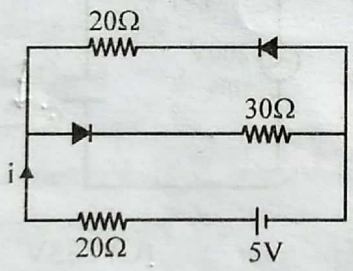
(A) The top surface of cube will become negatively charged

(B) The front surface of the cube will become positively charged

(C) The front surface of the cube will become negatively charged

(D) Both top and front surface of cube will become positively charged

22. Current in the circuit will be -

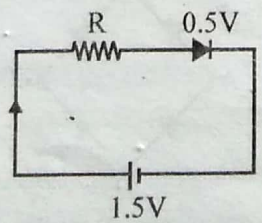


$20+30=50=R$.

$\frac{50}{5}=10=i$

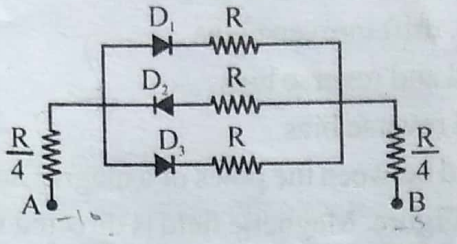
(A) $\frac{5}{40}$ A (B) $\frac{1}{10}$ A (C) $\frac{5}{10}$ A (D) $\frac{5}{20}$ A

23. The diode used in the circuit shown in the figure has a constant voltage drop of 0.5 V at all currents and a maximum power rating of 100 milliwatts. What should be the value of the resistor R connected in series with the diode for obtaining maximum current -



(A) 1.5 Ω (B) 5 Ω (C) 6.67 Ω (D) 200 Ω

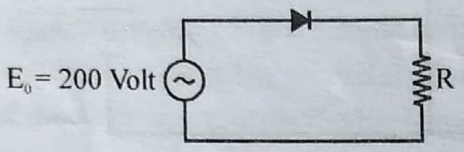
24. In the following circuits PN-junction diodes D_1, D_2 and D_3 are ideal for the following potential of A and B, the correct increasing order of resistance between A and B will be -



(i) –10V, –5V, (ii) –5V, –10V (iii) –4V, –12V

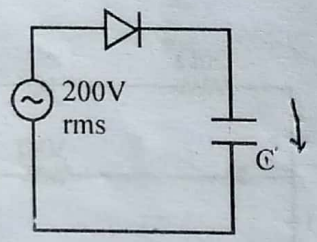
(A) (i) < (ii) < (iii) (B) (iii) < (ii) < (i) (C) (ii) = (iii) < (i) (D) (i) = (iii) < (ii)

25. A sinusoidal voltage of peak value 200 volt is connected to a diode and resistor R in the circuit shown so that half wave rectification occurs. If the forward resistance of the diode is negligible compared to R then rms voltage (in volt) across R is approximately -



(A) 200 (B) 100 (C) $\frac{200}{\sqrt{2}}$ (D) 280

26. In the figure, an A.C. of 200 rms voltage is applied to the circuit containing diode and the capacitor and it is being rectified. The potential across the capacitor C in steady state will be :-

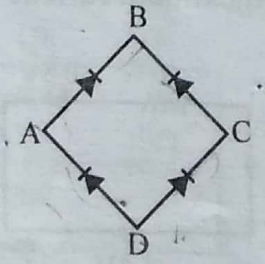


(A) 500V (B) 200V (C) 283V (D) 141V

27. For half wave rectifier if load resistance R_L is 2kΩ and P–N junction resistance R_d is 2kΩ determine rectification efficiency.

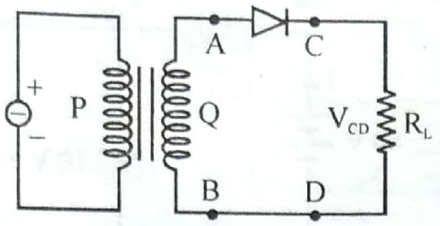
(A) 40.6 % (B) 20.3 % (C) 10.15 % (D) 81.2 %

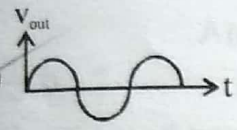
28. In the diagram, the input is across the terminals A and C and the output is across the terminals B and D, then the output is -

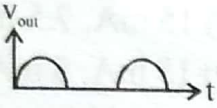


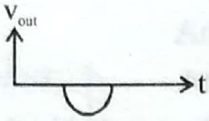
(A) zero (B) same as input (C) full wave rectifier (D) half wave rectifier

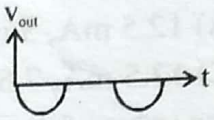
29. In the half-wave rectifier circuit shown. Which one of the following wave forms is true for V_{CD}, if the input is as shown?



(A) 

(B) 

(C) 

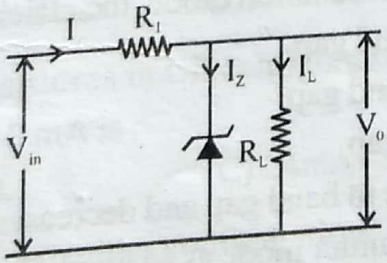
(D) 

30. Zener diode is a p-n junction which has -
(A) p-end heavily doped, n-end lightly doped
(B) n-end heavily doped, p-end lightly doped
(C) both p and n-ends heavily doped
(D) both p and n-ends lightly doped

31. Zener diode has both p and n-ends heavily doped so that -
(A) it has small thickness of depletion region
(B) it has large thickness of depletion region due to large recombination
(C) it has large reverse bias voltage
(D) it has weak reverse current when reverse biased

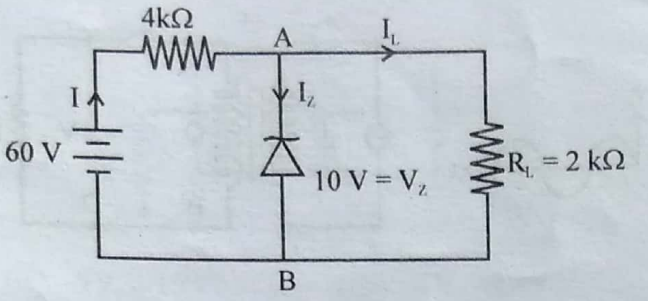
32. Most important use of zener diode is to have –
(A) constant voltage across applied load
(B) any desired current at constant voltage
(C) a p-n junction working under constant regulated voltage conditions
(D) a p-n junction to operate at high voltages

33. In given figure when input voltage increases,



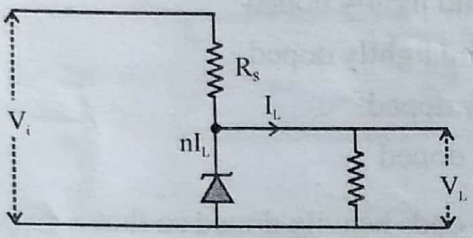
(A) the current through R_S, R_L and zener increases
(B) the current through R_S increases, zener increases but through R_L remains constant
(C) the current through R_S increases, through zener decreases, R_L increases
(D) the current through R_S increases, through zener remains constant but R_L increases

34. A Zener diode is connected to a battery and a load as shown below. The currents I, I_Z and I_L are respectively. **(JEE-Main Online-2014)**



(A) 12.5 mA, 5 mA, 7.5 mA
(B) 15 mA, 7.5 mA, 7.5 mA
(C) 12.5 mA, 7.5 mA, 5 mA
(D) 15 mA, 5 mA, 10 mA

35. The value of the resistor, R_S, needed in the dc voltage regulator circuit shown here, equals :- **(JEE-Main Online-2015)**



(A) $(Vi-V_L)/nI_L$ (B) $(Vi+V_I)/n\ I_L$ (C) $(V_i+V_L)/(n+1)\ I_L$ (D) $(V_i-V_L)/(n+1)I_L$

36. An experiment is performed to determine the I–V characteristics of a Zener diode, which has a protective resistance of R = 100 Ω, and maximum power of dissipation rating of 1 W. The minimum voltage range of the DC source in the circuit is :- **(JEE-Main Online-2016)**

(A) 0–24 V (B) 0–12 V (C) 0–8 V (D) 0–5 V

37. In a light emitting diode

(A) The intensity of emitted light increases with increase in forward current
(B) The intensity of emitted light increases with small increase in forward current and decreases after that
(C) The intensity of emitted light decreases with small increase in forward current and increases after that
(D) The intensity of emitted light decreases with increases in forward current

38. In the case of a solar cell using PN Junction diode, the efficiency of cell

(A) Increases with increase in band gap
(B) Increases with decrease in band gap
(C) Does not change with band gap
(D) Increases with small increase in band gap and decreases for large increase in band gap

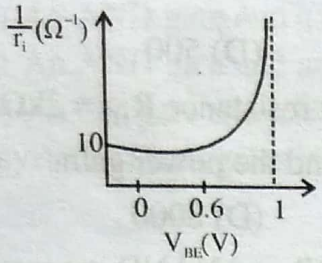
39. A transistor is used in common emitter mode as an amplifier, then:

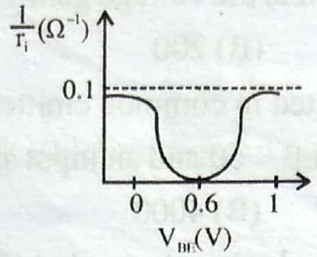
(1) the base emitter junction is forward biased
(2) the base emitter junction is reverse biased
(3) the input signal is connected in series with the voltage applied to bias the base emitter junction
(4) the Input signal is connected is series with the voltage applied to bias the base collector junction

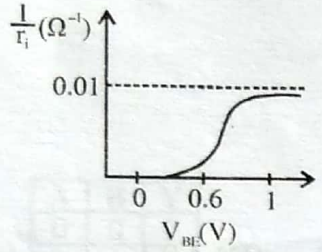
which is correct-

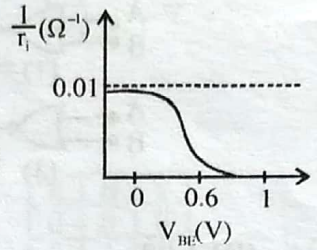
(A) 1, 2, 3 (B) 1, 2, 3, 4 (C) 1, 3 (D) 2, 3, 4

40. A realistic graph depicting the variation of the reciprocal of input resistance in an input characteristics measurement in a common emitter transistor configuration is : **(JEE-Main Online-2016)**

(A) 

(B) 

(C) 

(D) 

41. For CE configuration of a transistor-

(A) input resistance is very large while output resistance is very small

(B) input resistance is very small while output resistance is very high

(C) both input and output resistances are very small

(D) both input and output resistances are very large

42. In a n-p-n transistor circuit the collector current is 10 mA. If 90% of the electron emitted reach the collector then -

(A) the emitter current will be 9 mA (B) the base current will be 9 mA

(C) the emitter current will be 11 mA (D) the base current will be -1 mA

43. n-p-n transistors are preferred to p-n-p transistors because -

(A) they have low cost (B) they have low dissipation energy

(C) they are capable of handling large power (D) electrons have high mobility than holes.

44. When npn transistor is used as an amplifier **[AIEEE-2004]**

(A) electrons move from collector to base (B) holes move from emitter to base .

(C) electrons move from base to collector (D) holes move from base to emitter

45. For a transistor, α is 0.8. The transistor is in CE configuration. The change in the collector current when the base current changes by 6 mA is :-

(A) 6 mA (B) 4.8mA (C) 24mA (D) 8mA

46. A transistor is connected in common emitter configuration. The collector emitter voltage is 8V and load resistance of 800Ω is connected in the collector circuit. The voltage drop across the load resistance is 0.5V. If the current gain be 0.96, what is the base current :-

(A) 5 μA (B) 8 μA (C) 9.6 μA (D) 26 μA

47. What is the voltage gain in a common-emitter amplifier, where input resistance is 3Ω and load resistance 24Ω? Take $\alpha = 0.6$:-

(A) 8.4 (B) 4.8 (C) 2.4 (D) 12

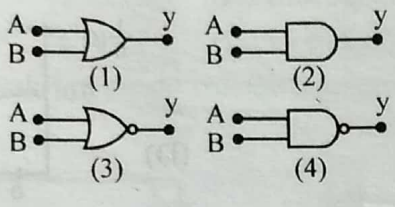
48. In a silicon transistor the base current is changed by 20 μA and this changes the emitter base voltage by 0.02 V and the collector current changes by 2mA. If the transistor is used as an amplifier with load resistance 5 kΩ, what is the voltage gain ?

(A) 100 (B) 200 (C) 250 (D) 500

49. A transistor, connected in common emitter configuration, has input resistance $R_{in} = 2k\Omega$ and load resistance of 5kΩ. If $\beta = 60$ and an input signal 12 mV is applied, find the power gain.

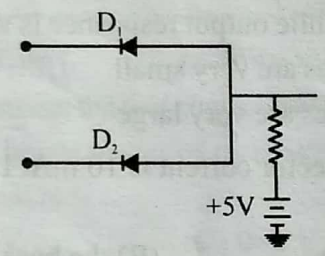
(A) 9000 (B) 4000 (C) 6000 (D) 8000

50. Given below are four logic gate symbol (figure). Those for OR, NOR and NAND are respectively



(A) 1,4,3 (B) 4,1,2 (C) 1,3,4 (D) 4,2,1

51. With the help of the arrangement shown in figure which of the following gates could be realised?



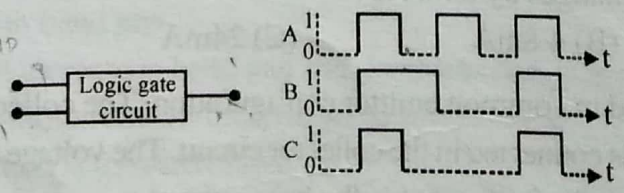
(A) OR (B) NAND (C) AND (D) NOR

52. The following truth table corresponds to the logic gate -

A	0	0	1	1
B	0	1	0	1
X	0	1	1	1

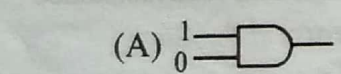
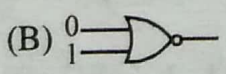
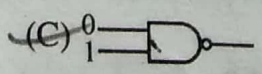
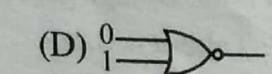
(A) NAND (B) OR (C) AND (D) XOR

53. The following figure shows a logic gate circuit with two input A and B output C. The voltage waveforms of A, B and C are as shown in second figure below. The logic gate is :

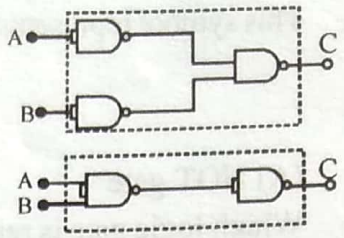


(A) OR gate (C) NAND gate (B) AND gate (D) NOR gate

54. Which of the following gates will have an output of 1 -

(A)  (B)  (C)  (D) 

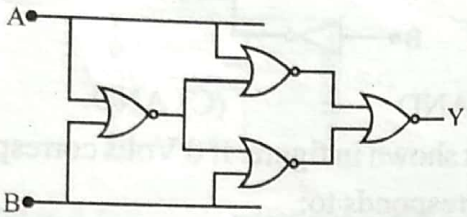
55. The combination of 'NAND' gates shown here under (figure) are equivalent to -



(A) An OR gate and an AND gate respectively
(B) An AND gate and a NOT gate respectively
(C) An AND gate and an OR gate respectively
(D) An OR gate and a NOT gate respectively

56. A system of four gates is set up as shown.The 'truth table' corresponding to this system is :-

(JEE-Main Online-2013)



(A)

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

(B)

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

(C)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

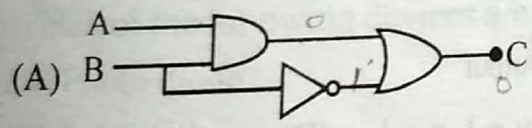
(D)

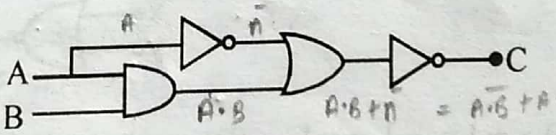
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

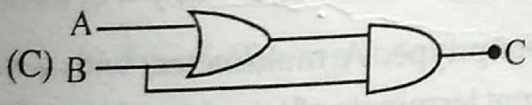
57. Which of the following circuits correctly represents the following truth table ?

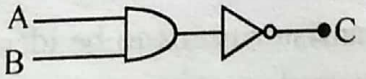
(JEE-Main Online-2013)

A	B	C
0	0	0
0	1	0
1	0	1
1	1	0

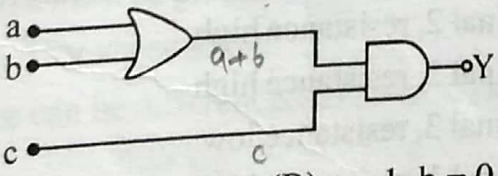
(A)


(B)


(C)


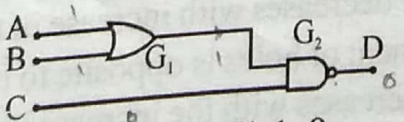
(D)


58. To get an output of 1 from the circuit shown in figure the input must be :- **(JEE-Main Online-2016)**



(A) a = 1, b = 0, c = 1
(B) a = 1, b = 0, c = 0
(C) a = 0, b = 1, c = 0
(D) a = 0, b = 0, c = 1

59. For the given combination of gates, if the logic states of inputs A, B, C are as follows A = B = C = 0 and A = B = 1, C = 0 then the logic states of output D are -



(A) 0, 0
(B) 0, 1
(C) 1, 0
(D) 1,1